Communication Department

Microcomputer Systems - First Exam, Fall 2018/2019 Student Name: Student No: Date: 18/11/2018 **Answer All Questions** (3 Questions, 3 pages): ------Q1------Q1-A: [24] Choose the correct answer: 1: The microprocessor is a microcomputer system in a single chip.] True 1 False 2: CISC processors are normally have l a large number of instructions.] a simple design. l a small number of transistors. 3: Harvard architecture uses shared data and address bus to access both data and program memory.] True] False ſ 4: The ATmega328p has KByte of on chip SRAM. 14 18 5: The general purpose registers in the ATMega328p are bit wide. 116 132 6: Which register of AVR microcontrollers hold the address of instruction to be fetched?] X register] PC register] Instruction register] R0 register 7: Which section of the CPU is responsible for performing addition? 1 Instruction Decoder 1 SFR 1 ALU 8: The flag is set whenever the result is too large. 1 C Flag 1 N Flag] V Flag] H Flag ſ 9: The flag is set after the addition of 0x37 and 0x2A.] N Flag] C Flag] V Flag] H Flag 10: The width of program memory address bus in AVR MCU is dependent on] Width of ALU Number of IO Lines] Width of Program Counter ſ 1 Size of SRAM 11: The more address pins, the more memory locations are inside memory. 1 True 1 False 12: memory can be erased using electrical signal.] SRAM 1 PROM 1 EPROM 1 EEPROM 13: In the, data at any memory location is addressed by a 16 bit pointer register.] Immediate addressing mode Direct addressing mode [Indirect addressing mode 14: The instruction is used to store an immediate number on GPR register.

] LDI

1 MOV

1ST

| 15: used to drive and control the direction of the line of | ction of DC-Motor. [] H-bridge circuit |
|--|---|
| [] Transistor | [] None inverting amplifier |
| 16: To set all pins of port B as input IO lines, you | must |
| [] Clear all bits of DDRB register | [] Set all bits of DDRB register |
| [] Clear all bits of PINB register | [] Set all bits of PINB register |
| Q1-B: [12] Describe the "Assembly Error" f | or each instruction of the following: |
| 1. MOV R20 , 15 | |
| | |
| | |
| 2. INC R16, 1 | |
| | |
| | |
| 3. SUB 8, R10 | |
| | |
| | |
| 4. LDS R16, X | |
| | |
| | |
| 5. OUT R18 , PORTB | |
| | |
| C MOD D20 D1 | |
| 6. XOR R30 , R1 | |
| | |
| | |
| ` | Q2 |
| Q2-A: [16] Complete following statements: | |
| 1: AVR CPU consists of: | 2: The main parts of microcomputer are: |
| 1 | 1 |
| | |
| 2 | 2 |
| 3 | 3 |
| 4 | 4 |
| 4 | 4 |
| 3: Program memory of ATMega328p is organized | 4: The operation of PortC is programmed and |
| into 2 sections, which are: | controlled by 3 registers, which are: |
| 1 | 1 |
| 2 | 2 |
| | 3 |

| 30=0x02, R31=0x01 | , and the o | contents of | the first 4 b | oytes of SRA | AM are | SRAM 7 [0x100] [0x101] | |
|--------------------------|---------------|-------------|---------------|--------------|---|------------------------|------|
| own in "SRAM ta | | d the conte | nts of requi | red register | s after | [0x102] | 0x3 |
| ecution of the follow | | | | | | | 0x0 |
| Instructions | R16 | R17 | R28 | R29 | R30 | R3 | 31 |
| AND R28 , R17 | | | | | | | |
| CLR R29 | | | | | | | |
| LD R29, Z | | | | | | | |
| ADD R16, R17 | | | | | | | |
| COM R31 | | | | | | | |
| DEC R30 | | | | | | | |
| | | | 03 | | | | |
| | | | ~ | | | | |
| 1. EEPROM over | | _ | | | | | |
| 1. LEI KOM OVEI | SKAWI | •••••• | ••••• | ••••• | | •••••• | •••• |
| | | •••••• | | ••••• | •••••• | •••••• | •••• |
| 2. Mega AVR ove | r Tiny AVR: | ••••• | ••••• | | • | •••••• | •••• |
| | | | | | ••••• | •••••• | •••• |
| 3. Parallel over sec | quential proc | essor: | | ••••••• | | | •••• |
| | | | | | •••••• | ••••• | •••• |
| 3-B: [15] What is | the main fu | nction of: | | | | | |
| 1. Boot loader: | | | | | | | |
| | | | | | | | |

3. Signal Conditioning Circuit